Visweswaraiah Technological University

III Semester B.E. Degree Examination

Model Question Paper-II

Time: 3 Hours — **Logic Design** — **Max.Marks : 100**

Note: *1. Answer any FIVE full questions*

2. All questions carry equal marks

1. a) Prove the Demorgan's law $\overline{x+y} = \overline{x} \cdot \overline{y}$ using Boolean postulates and theorems. 6

   b) Determine the Minterm canonical formula of the following:

   $T(x,y,z) = \overline{x}\,y + \overline{z} + x\,y\,z$ 4

   c) Mention the different methods available for manipulating Boolean Formulas. Explain any three in detail. 10

2. a) Using algebraic procedure realize the Boolean expression

   $f(w,x,y,z) = \overline{w}\,z + w\overline{z}\,(x + \overline{y})$ using only nor gates. 6

   b) Show that $A \oplus B \oplus C \oplus D = \Sigma m(1,2,4,7,8,11,13,14)$ 6

   c) Given the function $T(w,x,y,z) = \Sigma m(1,3,4,5,7,8,9,11,14,15)$. Use Karnaugh map to determine the set of all prime implicants. Indicate essential prime implicants. Find three distinct minimal expressions for T. 8

3. a) Using the Quine_ McCluskey method and prime implicant table reductions, determine a minimal sum for the incomplete boolean function

   $f(w,x,y,z) = \Sigma\, m(3,4,5,7,10,12,14,15) + dc(2)$. 10

   b) Explain the procedure for loading a K-map using Map Entered Variable technique. Write the Map Entered Variable K-map for the boolean function

   $f(w,x,y,z) = \Sigma\, m(2,9,10,11,13,14,15)$ 10

4. a) Explain with the help of a circuit diagram the operation of a two input TTL nand-gate with three-state output. 8

   b) What is a Field Effect Transistor? Explain how to construct a resistor with the n-channel, enhancement type MOSFET. 6

   c) Explain the operation of a two input CMOS nor-gate with the help of a circuit diagram. 6

5. (a) Explain the construction of a master-slave J-K flip-flop. Give the benefits of master-slave flip-flops. (10 marks)

(b) Design the binary counters having the following repeated binary sequence. Use I/C flip-flops only :—

0, 4, 2, 1, 6 (10 marks)

6. (a) Give the Logic diagram of a 4-bit bidirectional Shift Register with parallel load capability and briefly explain its operations. (10 marks)

(b) Clearly distinguish between :

(i) Synchronous and Asynchronous circuits.

(ii) Combination and Sequential circuits.

(iii) A Latch and a Flip-flop. (10 marks)

7. (a) You are provided with 4 K × 4 RAM chips, decoders and any type of logic gates. You are also provided with 4 K × 8 ROM chips. Use item to design the following :—

(i) 16 K × 8 memory, starting from address 8000 H (RPM).

(ii) 8 K × 8 ROM, starting from address 0000 H. (10 marks)

(b) Explain all the operations in a DRAM cell. (10 marks)

8. Write short notes on any *four* of the following :—

(a) CARRY LOOK AHEAD ADDER.

(b) PLA'S.

(c) CDROM.

(d) Johnson counters.

(e) Error detecting codes. (4 × 5 = 20 marks)

4. a) Explain the operation of a two input TTL nand-gate with totem-pole output with a neat circuit diagram. 8

b) Enumerate the different TTL subfamilies. 6

c) Explain the operation of a two-input NMOS nor gate, with the help of a circuit diagram. 6

5. a) Explain a 4 – bit parallel adder with carry lookahead scheme. 10

b) Explain how two Binary numbers A and B can be compared using a 1-bit comparator network. 10

6. a) Implement the boolean expressions.
$f_1(x_2,x_1,x_0) = \sum m(1,2,4,5)$ and $f_2(x_2,x_1,x_0) = \sum m(1,5,7)$ with a decoder and two OR gates. 6

b) Implement the Boolean function $f(w,x,y,z) = \sum m(0,1,5,6,7,9,12,15)$ using 8-to-1 multiplexer. 6

c) Explain the different types of flipflops along with their truth table. Also explain the race-around condition in a flipflop. 8

7. a) Design the mod-6 synchronous binary counter having the following repeated binary sequance using clocked JK flipflops. 10
0,4,2,1,6,0,4,.....

b) Explain the Mealy model and Moore model of a clocked synchronous sequential network. 10

5X4 =20

8. Write shortnotes on:
a) Full subtractor
b) Fan-in and Fan-out
c) Universal Shift Register
d) Programmable Read Only Memories (PROMS)

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Reg. No. CS134

Third Semester B.E. Degree Examination, August 2001

C.S.E/ I.S.E

Logic Design

Time: 3 hrs.] Max Marks: 100

Note: *Answer any FIVE full questions.*
All questions carry equal marks.

1. Find the minimal SOPs and minimal POSs expressions for $f(w, x, y, z) = \sum(0, 2, 4, 9, 12, 15) + \sum_{\phi}(1, 5, 7, 10)$ (20 Marks)

2. Design full adder and full subtractor. Implement using gates. (20 Marks)

3 (a) Explain a 4-bit parallel adder with a look-ahead carry scheme. (10 Marks)

(b) Explain a 4-bit magnitude comparator in detail. (10 Marks)

4. (a) Explain different types of Flip-Flops along with their truth table. (10 Marks)

(b) Design a counter that has a repeated sequence of 06 states listed below. Give its state diagram

Sequence		
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

(10 Marks)

5. (a) Explain 4 bit shift register in detail and give its timing diagram (10 Marks)

(b) Explain Johnson Counter with its circuit diagram and timing diagram. Give its state diagram. (10 Marks)

6. (a) Explain the following terms

i) Memory Cell (ii) Memory Word
iii) Density (iv) Address (v) Access time (10 Marks)

(b) Explain general memory operations in detail. (10 Marks)

7. (a) What are the main advantages of flash memory over EPROMS? (4 Marks)

(b) Explain various ROM applications. (8 Marks)

(c) Explain internal organization of a 64×4 RAM. (8 Marks)

8. Write short notes on :

i) Quine-McClusky method ii) Decoders iii) Schmitt triggers iv) ROM architecture (20 Marks)

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(Pages 2)

THIRD SEMESTER B.E. (COMPUTER SCIENCE AND ENGINEERING) DEGREE EXAMINATION

LOGIC DESIGN

Time : Three Hours

Maximum : 100 Marks

Answer any **five** *full questions.*
All questions carry equal marks.

1. (a) Compare K-map and Quine-McCluskey methods for simplification of Boolean expressions. (5 marks)

   (b) Using Quine-McCluskey tabulation method, obtain the set of prime implicants for the function

   $$f(a, b, c, d, e) = \Sigma (4, 12, 13, 14, 16, 19, 22, 24, 25, 26, 29, 30) + \Sigma_{\phi} (1, 3, 5, 20, 27).$$

   and hence obtain the minimal form of the given function, employing decimal representation. (15 marks)

2. (a) Using K-map simplify the following Boolean expression and give the implementation of the same using

   (i) NAND gates only.

   (ii) AND, OR and INVERT gates.

   $f(A, B, C, D) = \Sigma (2, 4, 8, 16, 31) + \Sigma_{\phi} (0, 3, 9, 12, 15, 18)$. (10 marks)

   (b) Using K-map obtain the simplified expression in (i) sum of products ; and (ii) product of sums form of the function

   $$f(A, B, C, D) = (A' + B' + C' + D') (A' + B' + C + D') (A + B' + C + D') (A + B + C + D') (A + B + C + D).$$

   (10 marks)

3. (a) Give the truth table for half-adder and full-adder. Develop the simplified expression for sum and carry of a full adder and realize the full-adder using only half-address. (10 marks)

   (b) Design a Excess-3 code to BCD-converter using NAND gates only. (10 marks)

4. (a) Given 3×8 decoder D, show the construction of a 4×16 decoder. (5 marks)

   (b) With a neat diagram, explain the internal logic construction of a 32×4 ROM. (10 marks)

   (c) List the PLA table for the BCD-to-excess-3 code converter. (5 marks)

Turn over

4/8

5. a) Explain the operation of a single decade BCD Adder in detail. 8
   b) Implement a full adder circuit with a decoder and two OR gates. 6
   c) What is an Encoder? Explain an 8-to-3 line Encoder. 6

6. a) Implement the following Boolean function with a multiplexer. 8

   $f(A, B, C, D) = \Sigma m (0,1,3,4,8,9,15)$

   b) Implement the following Boolean expression using a PROM.

   $f_1(x_2,x_1,x_0) = \Sigma m (0,1,2,5,7)$ 6

   $f_2(x_2,x_1,x_0) = \Sigma m (1,2,4,6)$ 6

   c) Explain the operation of a Master-Slave JK Flipflop.

7. a) Design a synchronous mod-8 counter with the following binary sequence: 10

   0,1,3,2,6,4,5,7 and repeat. Use clocked SR Flipflops.

   b) Explain how excitation tables, state tables and state diagrams are used in the analysis of a clocked synchronous sequential network. 10

5X4 = 20

8. Write short notes on:
   a) Shannon's reduction theorems
   b) Petrik's method of determining Irredundant Expressions
   c) Binary Ripple Counter
   d) Programmable Logic Arrays (PLAS)

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Visweswaraiah Technological University

III Semester B.E. Degree Examination

Model Question Paper-I

Time: 3 Hours — **Logic Design** — **Max.Marks : 100**

Note: *1. Answer any FIVE full questions*

2. All questions carry equal marks

1. a) Prove the following using Boolean postulates.

   i) $xy + yz + \overline{x}\,z = xy + \overline{x}\,z$

   ii) $(x+y)(y+z)(\overline{x}+z) = (x+y)(\overline{x}+z)$ 6

   b) Show that $T(x,y,z) = (x+y\ \overline{(\overline{x}(\overline{y}+\overline{z}))}) + \overline{x}\ \overline{y} + \overline{x}\ \overline{z} = 1$ 6

   c) State the Shannon's reduction theorems. Simplify

   $f(w,x,y,z) = x + \overline{x}\ \overline{y} + \overline{w}\ \overline{x}(w+z)(y+\overline{w}\,z)$ using the above theorems. 8

2. a) What are universal gates? Realize NOT, OR and AND functions using universal gates. 6

   b) Using graphical procedure, obtain a nand-gate realization of the boolean expression

   $f(w,x,y,z) = \overline{w}\,z + w\,\overline{z}(x+\overline{y})$ 6

   c) Using Karnaugh maps, determine the minimal sums and minimal products for

   $f(w,x,y,z) = \Pi M(1,4,5,6,11,12,13,14,15)$

   Is your answer unique? 8

3. a) Using Quine_McCluskey and Petric methods, determine all the irredundant distinctive normal formulas for the following boolean function. Indicate which expressions are minimal sums.

   $f(w,x,y,z) = \sum m(4,5,7,12,14,15)$ 10

   b) Consider the following Boolean equation: 10

   $T = f(w,x,y,z) = \sum m(2,4,5,10,11,14) + \sum dc(7,8,9,12,13,15)$

   Simplify T using a three variable Map Entered Variable K-map. Assign z to be the MEV.

3–Feb (Pages 2) CSL-34

THIRD SEMESTER B.E. (COMPUTER SCIENCE AND ENGINEERING) DEGREE EXAMINATION, MARCH 2001

LOGIC DESIGN

me : Three Hours Maximum : 100 Marks

Answer any **five** *questions.*
Draw neat diagrams for necessary questions.

1. (a) Using K-map, simplify the following Boolean expressions and give circuit implementation of the same using

   (i) NAND gates only (SOP form)

   (ii) NOR gates only (POS form)

   $f(A, B, C, D) = \sum (0, 1, 2, 4, 5, 12, 14) + d(8, 10)$.

   (5 + 5 = 10 marks)

   (b) Design BCD to 8, 4, – 2, – 1 code converter by using K-map method and implement the circuit by using AND–OR–INVERT gates only.

   (10 marks)

2. (a) Explain the differences between Combinational logic circuit and Sequential logic circuit.

   (4 marks)

   (b) Using Quine McClusky method, obtain the set of prime implicants for the given function

   $f(A, B, C, D, E) = \sum (0, 4, 5, 6, 7, 8, 12, 13, 14, 15, 16, 24, 29, 31) + d(21, 23)$

   and hence obtain minimal form of given function, employing decimal representation. Implement same by using NAND gates only.

   (16 marks)

3. (a) Design a combinational logic circuit whose input is a 4-bit binary number and whose output is the 2's complement of the input number. Implement by using suitable logic.

   (10 marks)

   (b) Show that $A \odot B \odot C \odot D = \sum (0, 3, 5, 6, 9, 10, 12, 15)$.

   (5 marks)

   (c) Give logic diagram and functions of pins for IC 74 LS 138. (5 marks)

4. (a) Implement BCD to Excess–3 code converter by using 4 bit parallel binary adder MSI chip (74 LS 283).

   (5 marks)

   (b) Explain with neat sketch working of decimal to BCD encoder. (5 marks)

   (c) What is a multiplexer ? With neat sketch, describe 4 : 1 multiplexer. Implement the given Boolean functions by using multiplexer chip.

   $f_1(A, B, C) = \sum (1, 2, 4, 7)$

   $f_2(A, B, C) = \sum (3, 5, 6, 7)$

   (10 marks)

Turn over

5. (a) Explain working of basic S-R FF by using NOR gates only. (4 marks)

(b) What is race around condition in FF ? Discuss in brief. (4 marks)

(c) Design mod-6 synchronous counter by using J-K FF. Give excitation table of FF, state diagram, state table and waveforms for same. (12 marks)

6. (a) Give logic diagram of MSI decade counter chip. Implement Mod 50 counter by using same chip. (5 marks)

(b) Explain with neat waveform working of 4-bit shift register. Modify same as Johnson's counter. (10 marks)

(c) Explain working of clock circuit by using Schmitt trigger. Design clock generator by using IC 74 LS 14 with output frequency of 2 kHz. (5 marks)

7. (a) With neat diagram, explain and differentiate static and dynamic RAM memory cell. (8 marks)

(b) Discuss 4 × 4 ROM by using diode matrix. (4 marks)

(c) Design following by using the memory chips, logic gates and decoders. Available memory chip 2 K × 4 bits RAM and 2 K × 8 bits ROM :—

(i) 8 K × 8 ROM with starting address 0000H.

(ii) 8 K × 8 bits RAM with starting address 2000H. (8 marks)

8. Write short notes on :

(a) PROM.

(b) Programmable logic device.

(c) Monostable multivibrator.

(d) BCD adder. (4 × 5 = 20 marks)

38/C

Reg. No. | | | | | | | | | | |

Third Semester B.E. Degree Examination, July/August 2002

Computer Science /Information Science and Engineering

Logic Design

Time: 3 hrs. [Max.Marks : 100

Note: Answer any FIVE full questions.
Draw figures wherever necessary.

1. (a) Using k-map, obtain simplified expression in sum of products.

$$f(A, B, C, D) = \Sigma(7, 9, 10, 11, 12, 13, 14, 15)$$ (8 Marks)

(b) Simplify the following Boolean function by tabulation method.

$$f(A, B, C, D) = \Sigma(0, 1, 2, 8, 10, 11, 14, 15)$$ (12 Marks)

2. (a) Simplify the Boolean function F using the dont care conditions d, in (1) Sum of products (2) Product of sums

$$F = A'B'D' + A'CD + A'BC$$

$$d = A'BC'D + ACD + AB'D'.$$ (10 Marks)

(b) Implement the following function with no more than two NOR gates. Assume that both normal and complement inputs are available.

$$F = A'B'C' + AB'D + A'B'CD'$$

$$d = ABC + AB'D'$$ (10 Marks)

3. (a) Implement a full subtractor with two half subtractors and an OR gate. (10 Marks)

(b) With suitable K-maps and logic diagrams design a code converter that converts BCD-to-excess-3 code converter. (10 Marks)

4. (a) Design a circuit that compares two 4-bit numbers A and B, to check if they are equal. The circuit has one o/p x, so that x=1 if A=B and x=0 if A≠ B. (5 Marks)

(b) Implement a full adder circuit with a decoder and two OR gates. (5 Marks)

(c) Implement the following function, with an 8 × 1 multiplexer, with A, B and D connected to selection line S_2, S_1 and S_0 respectively.

$$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$$ (10 Marks)

5. (a) Explain the operation of clocked JK Flip Flop with AND and NOR gates with relevant characteristic table and equation. (10 Marks)

(b) Design a counter with the following binary sequence 0,1,3,7,6,4 and repeat using T-F/F. (10 Marks)

6. (a) Design a serial adder using sequential logic procedure. (10 Marks)

Contd.... 2

(b) Explain the 4-bit binary ripple counter with state diagram, timing diagram and logic diagram using J-K, F/F that triggers on -ve edge. (10 Marks)

7. (a) How many address inputs, data inputs and data outputs are required for a $16K \times 12$ memory? What is its capacity in bytes? (4 Marks)

(b) Explain Flash memory? What are the advantages of flash memory over EPROM and EEPROMs. (6 Marks)

(c) Explain SRAM and DRAM. (10 Marks)

8. Write short notes on any FOUR of the following:

(a) Race around condition

(b) Schmitt triggers

(c) Johnson counter

(d) ROM architecture

(e) Error detecting codes. (20 Marks)

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CSI34

Reg. No. | | | | | | | | | |

Third Semester B.E. Degree Examination, January/February 2003

Computer Science /Information Science and Engineering

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Compare K-map and Quine-Mccluskey methods for simplification of Boolean expressions. Discuss their merits and demerits. (10 Marks)

   (b) Given the function $T(w,x,y,z) = \Sigma(1,3,4,5,7,8,9,11,14,15)$.

   Use K-map to determine the set of all prime implicants. Indicate essential prime implicants. Find three distinct minimal expressions for T. (10 Marks)

2. (a) Using tabulation method, determine the set of prime implicants for the function

   $f(w,x,y,z) = \Sigma(0,1,2,5,7,8,9,10,13,15)$

   and hence obtain the minimal form of the given function, employing decimal notation. (10 Marks)

   (b) Implement the following function with i) NAND gates ii) NOR gates use only four gates. Only normal inputs are available.

   $F = W^1xz + W^1yz + x^1yz^1 + Wxy^1z$
   d = Wyz. (10 Marks)

3. (a) Design a full adder. Give the truth table, simplified expressions and circuit diagrams. (6 Marks)

   (b) Design a combinational logic circuit whose input is a 4-bit binary number and whose output is the 2's complement of the input number. Implement by using suitable gates. (8 Marks)

   (c) Show that $A \odot B \odot C \odot D = \Sigma(0,3,5,6,9,10,12,15)$ (6 Marks)

4. (a) Explain a 4-bit parallel adder with carry look ahead scheme. (8 Marks)

   (b) Implement the following function with a multiplexer.

   $F(A,B,C,D) = \Sigma(0,1,3,4,8,9,15)$ (6 Marks)

   (c) List the PLA table for the BCD to excess-3 code converter. (6 Marks)

5. (a) Explain different types of flip-flops along with their truth table. Also explain the race-around condition in a flip flop. (10 Marks)

   (b) Design the mod-5 synchronous binary counter having the following repeated binary sequence using J-K filp flops.

   0, 4, 2, 1, 6, 0, 4... (10 Marks)

Cont.i.... 2

6. (a) Write the logic diagram of a 4 bit bidirectional shift register with parallel load capability and briefly explain its operations. (10 Marks)

   (b) Explain Johnson counter with its circuit diagram, timing diagram and state diagram. (10 Marks)

7. (a) With the help of a neat block diagram, briefly discuss the CPU-memory connections. List the steps that takes place when the CPU

   i) Reads from memory ii) writes into memory. (10 Marks)

   (b) Explain the different types of read only memories. Give at least three applications of ROMs. (10 Marks)

8. Write short notes on :

   i) 4-bit magnitude comparator

   ii) Schmitt trigger

   iii) BCD adder

   iv) Flash memory (5×4=20 Marks)

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CSI34

USN

Third Semester B.E. Degree Examination, July / August 2003

Computer Science /Information Science and Engineering

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *i) Answer any FIVE full questions.*
ii) Draw figures and truth tables wherever necessary
iii) All questions carry equal marks.

1. (a) Explain the grouping and simplification process in K - maps using the 3 - variable and 4- variable maps. (6 Marks)

   (b) Minimise the following using *K – maps*:-

   i) The S.O.P. expression is given by :-

   $$f(A,B,C,D) = \sum m(0,1,2,3,5,9,14,15) + \sum \Phi(4,8,11,12)$$

   ii) The P.O.S expression is given by

   $$f(A,B,C,D) = \pi M(0,1,2,5,8,9,10)$$

   Implement the minimal expressions thus obtained using basic gates (both normal and inverted inputs can be used) (14 Marks)

2. (a) List out the differences between combinational and sequential logic circuits. (4 Marks)

   (b) Determine the set of prime implicants for the given function :-
   $f(v,w,x,y,z) = \sum m(13,15,17,18,19,20,21,23,25,27,29,31)$
   $+ \sum \Phi(1,2,12,2,4)$ and obtain minimal expression. (16 Marks)

3. (a) Using truth table and K-map simplification, show the implementation of a FULL - ADDER is SOP. (10 Marks)

   (b) Using truth table and K - map simplification design a BCD to EXCESS - 3 code converter. Implement the code converter using BASIC GATES (only normal inputs can be used). (10 Marks)

4. (a) Implement in FULL - ADDER circuit using a 3 : 8 decoder and two OR - gates. (10 Marks)

   (b) Implement the Boolean function :

   $f(A,B,C,D) = \sum m(0,1,2,3,4,8,9,14,15)$ using an 8 : 1 MUX. (10 Marks)

5. (a) Using logic circuit. truth table and timing diagram explain the operation of a J-K flip-flop. Show the excitation table and the characteristic equation. (10 Marks)

   (b) Design a MOD - 12 asynchronous (ripple) up-counter using J-K. filp flops. Explain the operation briefly using timing - diagram. (10 Marks)

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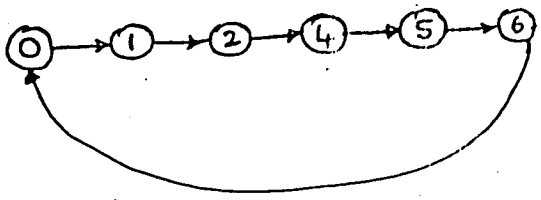
...ntd.... 2

6. (a) Design a counter that has a repeated sequence of SIX states as shown in the state diagram. Use J-K flip flops.



(10 Marks)

(b) With timing diagram and transition table, explain the operation of a 4 bit SISO shift register using D - flip flops. (10 Marks)

7. (a) Explain the principle of operation in EPROM and EEPROM. (10 Marks)

(b) Explain the principle of operation in SRAM and DRAM. (10 Marks)

8. Write short notes on ANY FOUR.

a) J-K master slave flip flop

b) Synchronous counters

c) Ring counter

d) Monostable multivibrator

e) PROM

(5×4=20 Marks)

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CS33

NEW SCHEME

USN

Third Semester B.E. Degree Examination, January/February 2004

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Explain the principle of duality. (4 Marks)

   (b) Mention two categories of Boolean expressions based on their structure. Write these forms for any give three - variable function $T(x, y, z)$. (8 Marks)

   (c) Give the Shanon's expansion theorem. (4 Marks)

   (d) Explain the exclusive-or-function. (4 Marks)

2. (a) Design an odd parity bit generator using gates for the decimal digits 0 to 9 represented in 84.21 BCD. Give the necessary truth table and draw the logic diagram. Explain. (8 Marks)

   (b) What code is used to label the row headings and column headings of a Karnaugh map and why? (4 Marks)

   (c) Using K-map obtain the minimal sum of products and the minimal product of sums form of the funciton $f(a, b, c, d) = \Sigma m(1, 2, 3, 5, 6, 7, 8, 13)$ (8 Marks)

3. (a) Mention one advantage and one disadvantage of the Quine-McCluskey method for obtaining the prime implicants of a given Boolean function. Obtain all the prime implicants of the function.

   $$f(v, w, x, y, z) = \Sigma m(4, 5, 9, 11, 12, 14, 15, 27, 30) + dc(1, 17, 25, 26, 31)$$

   Use Quinne-McCluskey method. Do you have any essential prime implicants. (12 Marks)

   (b) In what way MEV-K-map differs from the conventional K-maps? Simplify the function

   $$f(a, b, c, d) = \Sigma_m(2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$$

   using a two variable MEV-K-map. (8 Marks)

4. (a) With the aid of a neat circuit diagram explain the operation of a 2-input TTL nand gate with totem output. (8 Marks)

   (b) Discuss how a resistor could be constructed using MOSFET. Give the resister characteristics. (6 Marks)

   (c) Draw the NMOS as well as PMOS circuit diagrams to realise a NAND gate. Give the relevant truth tables. (6 Marks)

5. (a) Explain a 4 bit parallel adder with the carry look ahead scheme. Clearly indicate how this scheme improves the performance of the operation. (10 Marks)

   (b) With the aid of block diagrams clearly distinguish between a decoder and encoder. (4 Marks)

   (c) Give a 4-to-1 MUX implementation of the three variable function

   $f = \Sigma m(1, 4, 5, 7)$ (6 Marks)

Contd.... 2

6. (a) Illustrate how a PLA can be used for combinational logic design with reference to the functions.

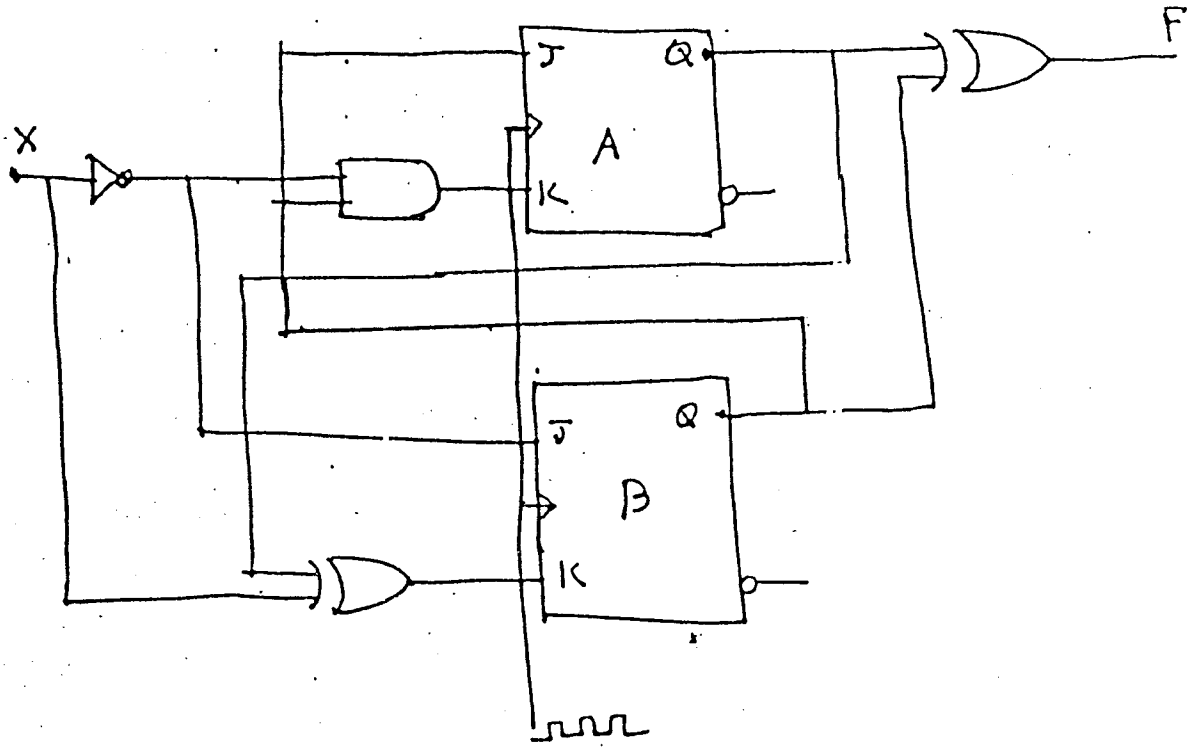
$$f_1(a,b,c) = \Sigma m(0,1,3,4)$$
$$f_2(a,b,c) = \Sigma m(1,2,3,4,5)$$

Realize the same assuming, that a 3 × 4 × 2 PLA is available. (10 Marks)

(b) Give the details of a master slave S-R flip flop. Draw the logic diagram. Explain the flip flop action during the control signal. Also give the function table. (10 Marks)

7. (a) Draw the block diagram of a mod-7 twisted ring counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states. (10 Marks)

(b) Construct the excitation table, transition table and state diagram for the Moore sequential circuit given below: (10 Marks)



8. Write notes on:
   (a) 1 - bit comparator
   (b) Fan - in and Fan out
   (c) Integration levels of IC's
   (d) Binary full subtractor.

(4 × 5=20 Marks)

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NEW SCHEME

CS33

USN

Third Semester B.E. Degree Examination, July/August 2004

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) State the principle of duality with an examples. (4 Marks)

   (b) Prove the following using Boolean theorems.

   i) $(x + \overline{x}\,\overline{y})\,(\overline{x} + \overline{y}) + yz = \overline{y} + z$

   ii) $\overline{w}\,\overline{y}\,\overline{z} + wz + \overline{y}z + xyz = \overline{w}\,\overline{y} + wz + xz$ (8 Marks)

   (c) Transform each of the following canonical expressions into its other canonical form in decimal notation.

   i) $f(x,y,z) = \Sigma m(1,3,5)$

   ii) $f(w,x,y,z) = \pi M(0,2,5,6,7,8,9,11,12)$ (8 Marks)

2. (a) What are universal gates? Realize the basic gates using them. (4 Marks)

   (b) Using graphical procedure, obtain a NOR - gate realization of the Boolean expression

   $$f(a,b,c,d) = \overline{a}d + a\overline{d}(B + \overline{C})$$

   Also explain the steps to be followed in the said procedure. (8 Marks)

   (c) Using K-map, determine the minimal sum of product expression and realize the simplified expression using only NAND gates.

   $$f(w,x,y,z) = \pi M(0,2,3,7,8,9,10)$$ (8 Marks)

3. (a) Using Quenie - McCluskey method and prime implicant reduction, determine the minimal SOP expression for the following using decimal notations.

   $$f(w,x,y,z) = \pi M(0,4,5,9) \bullet d(1,7,13)$$ (10 Marks)

   (b) Explain the procedure for loading a K-Map using Map entered variable technique with an example. (6 Marks)

   (c) For the following single variable entered map, obtain the minimal product of sum expression (4 Marks)

W\xy	00	01	11	10
0	Z	0	Z	1
1	Z	$\overline{Z}$	1	0

Fig. Q. No. 3(c)

Contd.... 2

4. (a) Explain a 2-input NAND gate TTL with Totem-pole output with a neat circuit diagram. (7 Marks)

   (b) What do you mean by FET? Describe the operation of a n-channel enhancement type MOSFET with neat diagrams. Write the circuit symbol for the same. (9 Marks)

   (c) Write the circuit diagram of a two input CMOS NAND gate. (4 Marks)

5. (a) Design a single decade BCD adder and explain the design methodology in detail. (8 Marks)

   (b) Implement a full subtracter using a decoder and two NAND gates. (6 Marks)

   (c) What is a comparator? Briefly explain the organisation of a 1-bit comparator. (6 Marks)

6. (a) Implement the following Boolean function using 8:1 multiplexer.
   $f(w,x,y,z) = \Sigma m(0,1,5,6,8,10,12,15)$ (6 Marks)

   (b) Using PROM realize the following expressions
   $f_1 = \Sigma m(0,1,3,5,7)$
   $f_2 = \Sigma m(1,2,5,6)$ (6 Marks)

   (c) Illustrate the use of PLA for combinational logic design with an example. (8 Marks)

7. (a) Design a mod-5 synchronous binary counter using clocked J-K flip-flops. (10 Marks)

   (b) Discuss how excitation tables, state tables and state diagrams are used to analyse a synchronous sequential network. (10 Marks)

8. Write short notes on :
   i) Incompletely specified functions
   ii) Irredundant conjunctive expressions
   iii) Network terminal behaviour
   iv) Race around condition. (4×5=20 Marks)

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NEW SCHEME

USN | | | | - | | | | | | |

Third Semester B.E. Degree Examination, January/February 2005

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Explain the principle of duality in Boolean algebra. Write the duals of the following Boolean theorems:
   i) $a + b + ab = a + b$
   ii) $a + b + \overline{a}\,\overline{b} = 1$
   iii) $ab + bc + \overline{c}a = bc + \overline{c}a$ (8 Marks)

   (b) Complement the following Boolean expressions and write them as the sum of minterms.
   i) $\overline{a} + \overline{b} + \overline{c} + \overline{d}$
   ii) $ab + \overline{(abcd)}$ (6 Marks)

   (c) Rewrite the following Boolean expressions in the M-notation and simplify :
   i) $(a + b)(a + c)$
   ii) $(a + b)(b + c)(\overline{c} + a)$ (6 Marks)

2. (a) What ia a universal gate? Consider a gate which takes two inputs A and B and produces an output $\overline{A} \cdot B$. Would you consider it a universal gate? Discuss. (10 Marks)

   (b) Get the minimised sum-of products expression for
   $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 8, 9)$
   with don't cares : $\sum m(10, 11, 12, 13, 14, 15)$
   Use Karnaugh map for simplification. (10 Marks)

3. (a) Give the truth table for a binary full adder function and obtain the irredundant disjunctive normal expression for the function. Show how the function could be realised using NAND gates. (10 Marks)

   (b) Use Quine McCluskey method and simplify the following function : $f(a, b, c, d) = \sum m(0, 1, 2, 3, 8, 9)$ (10 Marks)

4. (a) Explain the following properties of integrated circuits of the SSI type (small scale integration type)
   i) Propagation delay
   ii) Noise margin
   iii) Fan - in
   iv) Fan-out
   Compare TTL and CMOS gates, in respect of these properties. (10 Marks)

   (b) With a circuit diagram, explain the operation of the CMOS NAND gate. What are its advantages over corresponding TTL gates? (10 Marks)

Contd... 2

5. (a) Explain clearly the Totem pole output stage and the Three-state output stage of a TTL gate. When would the three state stage be useful? (10 Marks)

   (b) What is a look-ahead carry adder? Explain the circuit and operation of a 4-bit binary adder with look-ahead carry. (10 Marks)

6. (a) How would you realise the function

   $ABCD + \overline{A}BC + B\overline{C}\,\overline{D}$ using an 8-to -1 multiplexer? (10 Marks)

   2v (b) Distinguish between PLA and PAL. Show how you would realise a Boolean function using a PLA. (10 Marks)

7. (a) Explain the operation of a simple SR flip flop using NAND gates. (10 Marks)

   (b) Draw the circuit and explain a synchronous mod-6 counter using J-K flipflops. (10 Marks)

8. Design a sequential machine using D-flipflops for realising the state table below. The machine is of a single input single output type.

Present state	Next state for input x=		Output Z for input x=	
	0	1	0	1
A	B	C	0	0
B	A	A	0	1
C	D	A	0	1
D	A	D	0	1

Indicate the state transition diagram. Does the state assignment. Work out the excitation and the output logics? (20 Marks)

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No... 1

NEW SCHEME

USN | | | | | | | | | |

Third Semester B.E. Degree Examination, July/August 2005

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

[Max.Marks : 100

ne: 3 hrs.]

Note: *Answer any FIVE full questions.*

1. (a) Explain Demorgan's theorems in Boolean Algebra. (4 Marks)
   (b) State and explain two applications of shift register. (6 Marks)
   (c) Design a combinational circuit for 3 bit even-parity generator and implement it using NAND gates only. (10 Marks)

2. (a) Design BCD to Excess 3 code converter using NOR gates only. (8 Marks)
   (b) What is race around condition? Explain how it is eliminated using J-K master-slave flip-flop. (12 Marks)

3. (a) Using Quine Mc Clusky tabulation method, obtain the set of prime implicants for the function
   $$f(a,b,c,d) = \sum(0,1,4,5,9,10,12,14,15) + \sum\phi(2,8,13)$$
   and hence obtain the minimal form of the given function employing decimal representation. (12 Marks)
   (b) Design mod-4 ripple up counter with initial state is $(011)_2$. Draw timing diagram for the same. (8 Marks)

4. (a) Simplify the following using VEM technique. Reduce 4 variables to 3 variables
   $$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,C\overline{D} + A\,B\,C\,D + A\,B\,C\overline{D}$$
   Implement it using AOI logic. (8 Marks)
   (b) Define fan-in and fan out - (4 Marks)
   (c) Explain a two input NAND gate TTL with totem pole output with a neat circuit diagram. (8 Marks)

5. (a) Design 3:8 active low output decoder. (7 Marks)
   (b) Compare Moore and Meelay models. (8 Marks)
   (c) Construct 8:1 multiplexer using 2:1 multiplexer. (5 Marks)

6. (a) Implement the following multi Boolean function using $3 \times 4 \times 2$ PLA PLD
   $$f_1(a_2,a_1,a_0) = \sum m(0,1,3,5) \text{ and}$$
   $$f_2(a_2,a_1,a_0) = \sum m(3,5,7)$$ (8 Marks)
   (b) State Shannons expansion theorem and using this theorem expand the following expression
   $$f = \overline{b} + \overline{a}c$$ (4 Marks)

Cont.: 2

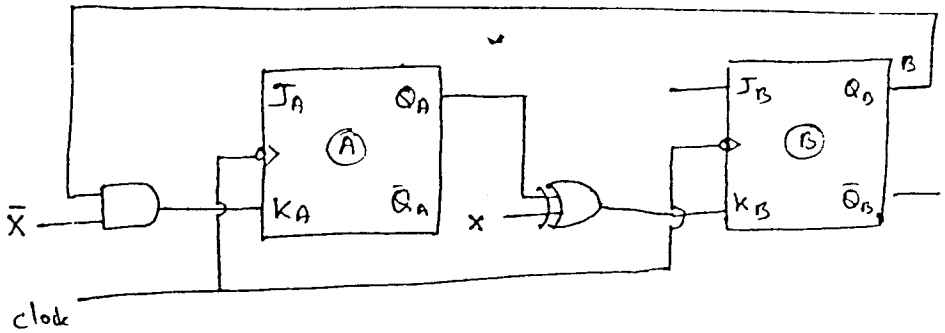
(c) Design a MOD - 4 synchronous down counter using JK flip flops and implement it. (8 Marks)

7. (a) Define and explain prime implicate. (5 Marks)

(b) Solve the following expression using Boolean algebra technique

$$F = \overline{\overline{A\overline{B} + A(\overline{\overline{A} + \overline{C}}) + \overline{A \oplus B}}}$$ (5 Marks)

(c) Derive transition table. State table and state diagram for moore sequential circuit shown in below figure. (10 Marks)



8. (a) Explain the working of a CMOS, NOT, NAND and NOR gates. (5 Marks)

(b) Implement the following multi-Boolean function using PROM PLD

$f_1(x_1, x_0) = \overline{x_1} + x_0$
$f_2(x_1, x_0) = x_1$ (4 Marks)

(c) $f(a, b, c, d) = \sum m(1, 2, 3, 5, 6, 7, 11, 12, 13, 14, 15)$
for the above expression

i) Draw the logic diagram using AOI logic for minimal sum. Obtain minimal sum using K-map.

ii) Find all the prime implicants and essential prime implicants. (8 Marks)

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CS33

USN

NEW SCHEME

Third Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / EE / IT / BM / ML / CS / IS
Logic Design

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Prove the following :
   i) $\overline{ac} + \overline{a}b + \overline{a}c + ab = a\overline{b}$
   ii) $(a+b)(\overline{ac}+c)(\overline{b}+ac) = \overline{a}b$
   iii) $a\overline{b} + b\overline{c} + \overline{a}c = \overline{a}b + \overline{b}c + a\overline{c}$ **(10 Marks)**

   b. Implement
   i) $w = x\overline{y} + \overline{x}y$ using NAND gates
   ii) $w = (x+z)(\overline{y}+\overline{v})(\overline{w}+\overline{x}+\overline{y})$ using NAND **(06 Marks)**

   c. Simplify using Boolean algebra **(04 Marks)**
   $\overline{w}x\overline{y}z + w\overline{x}\overline{y}z + xz + xy\overline{z}$

2 a. Identify all prime implicants and essential prime implicants of the following functions using K map.
   i) $f(a,b,c,d) = \Sigma m(0,1,2,5,6,7,8,9,10,13,14,15)$
   ii) $f(a,b,c,d) = \Pi m(0,2,3,8,9,10,12,14)$ **(08 Marks)**

   b. Find a minimal sum for the following Boolean function using Quine McCluskey method and prime-implicant table reduction **(12 Marks)**
   $f(a,b,c,d) = \Sigma m(3,4,5,7,10,12,14,15) + \Phi(2)$

3 a. Find the minimal sum and minimal product using MEV technique using a,b,c as map variables **(08 Marks)**
   $f(a,b,c,d) = \Sigma m(3,4,5,7,8,11,12,13,15)$

   b. Find minimal sum and minimal product for the following function using K-map **(08 Marks)**
   $f(a,b,c,d) = \Sigma m(6,7,9,10,13) + dc(1,4,5,11,15)$

   c. Define :
   i) Positive logic
   ii) Negative logic **(04 Marks)**

4 a. With diagram, define
   i) Rise time
   ii) Fall time
   iii) Propagation delay
   iv) Fan-in
   v) Fan out. **(10 Marks)**

   b. Using NMOS draw the circuit for
   i) Inverter
   ii) NOR gate
   iii) NAND gate **(06 Marks)**

   c. Draw the circuit diagram for
   i) 2-input CMOS NOR
   ii) 2-input CMOS NAND **(04Marks)**

Contd.... 2

5 a. Construct 16:1 multiplexer using 4 tol and 2 tol multiplexer. (04Marks)

b. Implement the following using 4×4 PROM

Input (a, b)		Output (f_0, f_1, f_2, f_3)			
0	0	0	0	1	1
0	1	0	1	0	0
1	0	0	1	0	0
1	1	1	1	0	0

(04 Marks)

c. Implement $f(a,b,c,d) = \Sigma m(0,1,5,6,7,9,10,15)$ using

i) 8:1 MUX with a,b,c as select lines (06 Marks)

ii) 4:1 MUX with a,b as select lines (06 Marks)

d. Design a 4 bit parallel fast look a head carry generator.

6 a. Design a synchronous counter using JK flip flops to count in the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 . . . . use state diagram and state table. (08 Marks)

b. Explain TTL with

i) Wired logic

ii) Open collector

iii) Totem pole output (12 Marks)

7 a. Give the logic diagram of

i) SR latch

ii) Gated D latch

iii) Master Slave JK flip flop (08 Marks)

iv) Master Slave SR flip flop (08 Marks)

b. With diagram explain universal shift register.

c. Explain the working of switch debouncer using SR latch. (04 Marks)

8 Write short notes on :

a. Ripple counter

b. PLA

c. Ring counter

d. Decoder. (20 Marks)

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USN | | | | | | | | | | |

06CS33

Third Semester B.E Degree Examination, Dec. 07 / Jan. 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions choosing at least TWO questions from each part..***

PART – A

1 a. Using Karnaugh map simplify the following Boolean expression and give the implementation of the same using :
i) NAND gates only (SOP form) ii) NOR gates only (POS form)
$f(A, B, C, D) = \sum m\ (0, 1, 2, 4, 5, 12, 14) + dc\ (8, 10)$. (08 Marks)

b. Find the prime implicantes for the Boolean expression using Quine Mc Clusky's method.
$F(w, X, Y, Z) = \sum m\ (1, 3, 6, 7, 8, 9, 10, 12, 13, 14)$. (10 Marks)

c. Explain the principle of duality. (02 Marks)

2 a. Realize the Boolean expression $f(w, x, y, z) = \sum m(4, 6, 7, 8, 10, 12, 15)$ using a 4 to 1 line multiplexer and external gates. (08 Marks)

b. Design a 1-bit comparator using basic gates. (05 Marks)

c. Implement the following Boolean functions using an appropriate PLA.
$F1(A, B, C) = \sum m(0, 4, 7)$; $F2(A, B, C) = \sum m(4, 6)$. (04 Marks)

d. What are the three different models for writing a module body in Verilog HDL. Give an example for any one model. (03 Marks)

3 a. Explain with example the 2's complement arithmetic using all the cases. (04 Marks)

b. Draw a block diagram of a 4 – bit adder – subtract circuit using full adder and give a brief description. (04 Marks)

c. Design a 2-bit fast adder. Give its implementation using gates. (08 Marks)

d. Write a HDL code for a full adder. (04 Marks)

4 a. Write the characteristic of an ideal clock. (06 Marks)

b. With the help of a block diagram, explain the working of a JK Master – Slave flip – flop. (08 Marks)

c. Show how a SR flip – flop can be converted to a JK flip – flop. (06 Marks)

PART – B

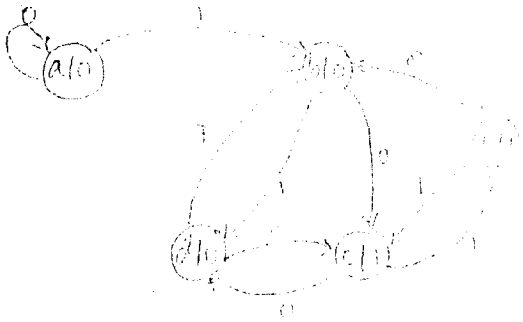
5 a. Distinguish between a ring counter and a Johnson counter. (04 Marks)

b. Explain the working of a 3-bit asynchronous down counter. (06 Marks)

c. Design a synchronous mod – 5 up counter using JK flip – flop. Give excitation table of JK flip – flop, state diagram and state table. (10 Marks)

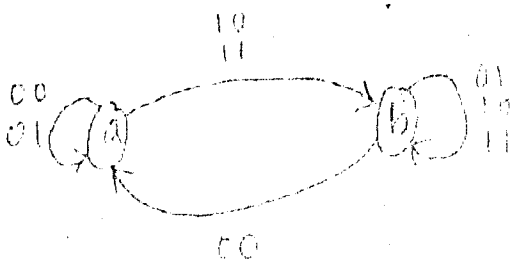
6 a. Explain the difference between Mealy and Moore models. (04 Marks)

b. Reduce the state transition diagram by row elimination method and implication table method.



(10 Marks)

c. Design an asynchronous sequential logic circuit for the state transition diagram shown. (06 Marks)



7 a. Draw a 4-bit D/A converter using R/2R resistors and explain its working. (10 Marks)

b. Explain the A/D converter by simultaneous conversion. Draw the block diagram of a 2 – bit simultaneous A/D converter. (10 Marks)

8 a. With the aid of a circuit diagram, explain the operation of a 2 – input TTL NAND gate with totem – pole output. (08 Marks)

b. Explain the operation of a 2 – input CMOS NOR gate with a help of a circuit diagram (06 Marks)

c. Write a note on the CMOS characteristics. (06 Marks)

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USN | | | | | | | | | | |

06CS33

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, choosing atleast two from each part.***

PART - A

1 a. What are universal gates? Implement the following function using universal gates only $\overline{(\overline{(A+B)C})D}$ (04 Marks)

b. Simplify the following using K – map $F(A,B,C,D) = \overline{A}\overline{B}C + AD + B\overline{D} + C\overline{D} + A\overline{C} + \overline{A}\overline{B}$. (06 Marks)

c. What are the drawbacks of k-map? Simplify the following expression using Quine – Mc Clusky Method. $F(A,B,C,D) = \Sigma(1,2,8,9,10,12,13,14)$. (10 Marks)

2 a. Show that using a 3 – to – 8 decoder and multi –input OR gate. The following Boolean expressions can be realized.
$F_1(A,B,C) = \Sigma m(0,4,6)$, $F_2(A,B,C) = \Sigma m(0,5)$, $F_3(A,B,C) = \Sigma m(1,2,3,7)$. (04 Marks)

b. Design Decimal – to – BCD encoder? (04 Marks)

c. What are the different types of PLD's and implement the 7 – segment decoder using PLA? (08 Marks)

d. Write a verilog code for 4 : 1 multiplexer using case statement. (04 Marks)

3 a. i) Perform 8 – bit addition of the decimal numbers – 28 and + 15 in 2's complement.
ii) Perform 8 – bit subtraction of the decimal numbers – 28 and + 65 in 2's complement. (06 Marks)

b. i) Find the binary addition of $(7510)_{10}$ and $(538)_{10}$ using 16 – bit numbers.
ii) Find the binary subtraction of $(200)_{10}$ and $(125)_{10}$ using 8 – bit numbers. (10 Marks)

c. Explain the binary Adder – subtracted circuit with an example. (04 Marks)

4 a. What is Schmitt trigger? Explain Schmitt trigger transfer characteristic. (10 Marks)

b. Explain the different types of flip fops along with their truth table. Also explain the race – around condition in a flip flop.

c. Differentiate between combinational circuit and sequential circuit. (10 Marks)

PART - B

5 a. Explain a 4 –bit serial input shift registers in detail and give its timing diagram. (10 Marks)

b. Design a mod – 5 synchronous up counter using JK flip flop. (10 Marks)

6 a. Explain Moore model with state synthesis table and also obtain the circuit diagram for Moore model. (10 Marks)

b. Design an asynchronous sequential logic circuit for state transition diagram shown in Fig. Q 6(b).

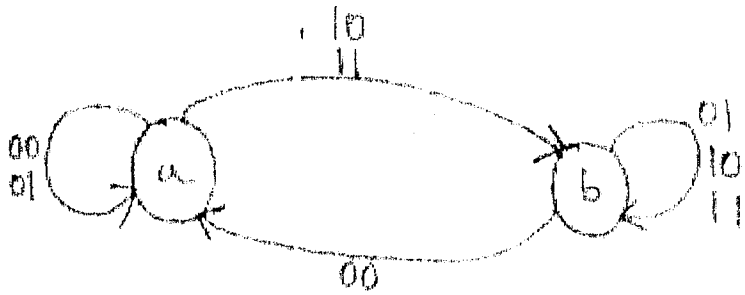

Fig. Q 6(b) (10 Marks)

7 a. What is a binary ladder? Explain the binary ladder with a digital input of 1000. (10 Marks)

b. Explain a 2 – bit simultaneous A/D converter. (10 Marks)

8 a. With a circuit diagram, explain the operation of the CMOS NAND gate. (10 Marks)

b. Explain a 2 – input NAND gate TTL with Totem – pole output with a neat diagram. (10 Marks)

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USN | | | | | | | | | | |

06CS33

Third Semester B.E. Degree Examination, Dec 08/Jan.09
Logic Design

Time: 3 hrs. Max Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. What are universal gates? Realize basic gates using only NAND gates. (05 Marks)

b. Simplify the following logic equation using Karnaugh map and give the implementation of the simplified expression. $F(A,B,C,D) = \Sigma m(7) + d(10,11,12,13,14,15)$ (05 Marks)

c. Give simplified logic equation using Quine-McClusky method for the following Boolean function. $F(A,B,C,D) = \Sigma m(0,1,2,3,10,11,12,13,14,15)$ (10 Marks)

2 a. Design a 32-to-1 multiplexer using two 16-to-1 multiplexer and one 2-to-1 multiplexer. (05 Marks)

b. Show how two 1-to-16 demultiplexers can be connected to get a 1-to-32 demultiplexer. (05 Marks)

c. Give 7-segment decoder using PLA. (05 Marks)

d. Give verilog HDL code for 4-to-1 multiplexer using conditional 'assign' and 'case' statements. (05 Marks)

3 a. Explain with an example of 2's complement arithmetic using all four cases. (04 Marks)

b. Design full – subtractor. (06 Marks)

c. What is ALU? Show how A>B and A ≥ B can be generated in IC 74181 ALU. (05 Marks)

d. What is fast adder? Give logic circuit for 2-bit fast adder. (05 Marks)

4 a. Explain monostable multi-vibrator with circuit diagram and waveform. (08 Marks)

b. Realize the sequencial circuit for the state diagram shown in Fig.4(b). (06 Marks)

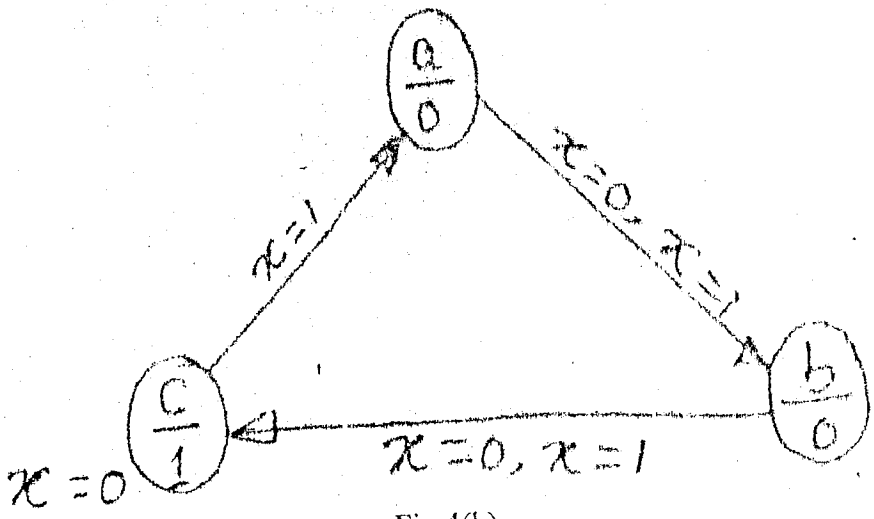

Fig.4(b)

c. Show how a SR-flip flop can be converted into a T-flip flop. (06 Marks)

PART – B

5 a. Explain 4-bit shift register of serial with timing diagram. (05 Marks)

b. Explain Ripple counter (Asynchronous counter) with truth table and waveform. (05 Marks)

c. Design a self-correcting modulo-6 counter as described in state sequence of Fig.5(c) in which all the unused state leads to state CBA= 000. (10 Marks)

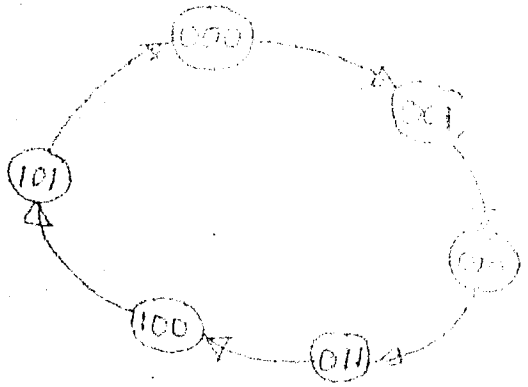

Fig.5(c)

6 a. A sequential circuit has one input and one output. The state diagram is shown in Fig.6(a). Design the sequential circuit with (i) D-flip flop (ii) T-flip flop. (10 Marks)

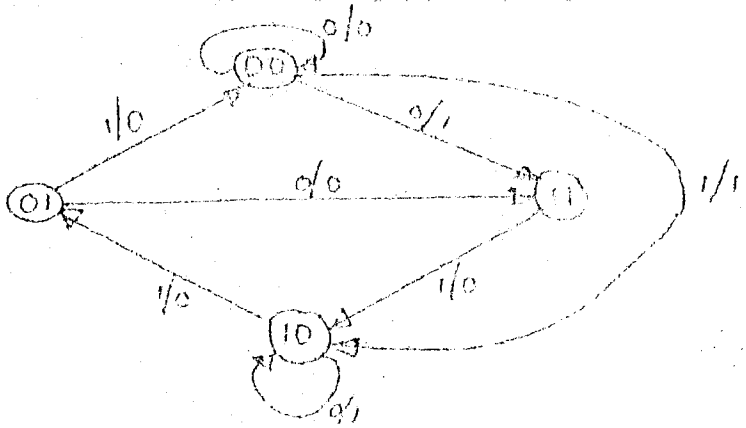

Fig.6(a)

b. Design mealy type sequence detector to detect a serial input sequence of 101. (10 Marks)

7 a. What is a binary ladder? Explain the binary ladder with a digital input of 1000. (10 Marks)

b. Explain with block diagram of successive approximation ADC. (06 Marks)

c. Explain accuracy and resolution for A/D converter. (04 Marks)

8 a. With the help of circuit diagram explain the operation of 2-input TTL-NAND gate. (08 Marks)

b. Explain the operation of a 2-input CMOS-NAND gate with the help of a circuit diagram. (06 Marks)

c. Give six comparisons of CMOS and TTL families. (06 Marks)

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06CS33

Third Semester B.E. Degree Examination, June-July 2009
Logic Design

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Write the truth table of the logic circuit having 3 inputs A, B & C and the output expressed as $Y = A\bar{B}C + ABC$. Also simplify the expression using Boolean Algebra and implement the logic circuit using NAND gates. (06 Marks)

b. What is the purpose of using an expander with an AND – OR – INVERT gate? Write a logic circuit of an expander driving expandable AND – OR – INVERT gate. (04 Marks)

c. Simplify the following logic expression using Karnaugh map and also by Quine – McClusky method.

$$f(A, B, C, D) = \sum m(1, 2, 8, 9, 10, 12, 13, 14)$$ (10 Marks)

2 a. Write the truth table of a 4-bit Binary to Gray code converter and realize the same using four 74151 ICs (8-to-1 multiplexer) (10 Marks)

b. Realize 7-segment decoder using PLA. (06 Marks)

c. Write Verilog code for a combinational logic circuit that compares two 4-bit numbers A and B and generates a 3-bit output Y. The 3 bits of Y represent A = B, A > B and A < B. (04 Marks)

3 a. Show the 8-bit subtraction of these decimal numbers in 2's complement representation
i) +68, – 43 ii) +16, – 38 (04 Marks)

b. What is a fast adder? Show how two IC 74283s can be connected to add two 8-bit numbers. (06 Marks)

c. What is an ALU? How A < B function is performed in IC 74181? Also, show how 7 can be subtracted from 13 using IC 74181. (10 Marks)

4 a. Draw carefully the waveforms at points A, B and C in Fig.4(a). (06 Marks)

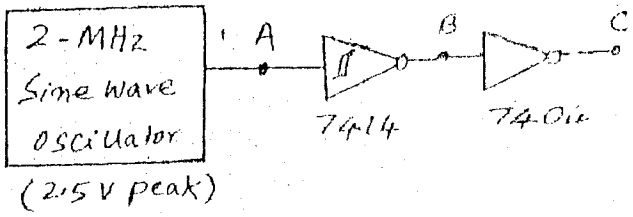

Fig.4(a)

b. Differentiate transparent and gated flip-flops. What are their applications? (04 Marks)

c. Show how to convert D flip-flop to JK flip-flop. (10 Marks)

PART – B

5 a. Name the four basic types of shift registers, and draw a block diagram for each. (04 Marks)

b. Draw the gates necessary to decode the 16 states of a mod-16 counter 7493. What are decoding glitches? How to eliminate them? (10 Marks)

c. What are presettable counters? What is lock out of a counter? Show how to construct a mod-13 counter using 74163 synchronous binary counter IC. (06 Marks)

6 a. Draw state transition diagram of a sequence detector circuit that detects '1101' from input data stream using both Mealy and Moore models. (1st Data bit = 1, 2nd data bit = 1, 3rd Data bit = 0 and 4th Data bit = 1). (08 Marks)

b. Design a parity generator using asynchronous sequential logic that gives output = 1 when it receives odd number of pulses and output = 0 if the number of pulses received is even. (08 Marks)

c. What are the problems with asynchronous sequential circuits? (04 M

7 a. What is accuracy and resolution of the D/A converter? What is the resolution of a 12-bit D/A converter which uses a binary ladder? If the full-scale output is +10V, what is the resolution in volts? (04 Marks)

b. Find the following for a 12-bit counter-type A/D converter using a 1-MHz clock:
   i) Maximum conversion time
   ii) Average conversion time
   iii) Maximum conversion rate (06 Marks)

c. Explain successive approximation A/D converter. (10 Marks)

8 a. Draw the circuit for a CMOS inverter and explain its working. (06 Marks)

b. Discuss the features of High-speed TTL, Low-power TTL and Schottky TTL families. (06 Marks)

c. Explain methods for interfacing CMOS devices to TTL devices (08 Marks)

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06CS33

Third Semester B.E. Degree Examination, Dec.09/Jan.10
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, choosing at least two from each part.***

PART-A

1 a. Implement $AB + \overline{C}\,\overline{D}$ with only three NAND gates. Draw logic diagram also. Assume inverted input is available. (06 Marks)

b. Reduce the following functions using K-map techniques.
i) $f(P,Q,R,S) = \Sigma m\,(0, 1, 4, 8, 9, 10) + d(2, 11)$
ii) $f(A,B,C,D) = \Pi m\,(0, 2, 4, 10, 11, 14, 15)$. (06 Marks)

c. Reduce the following function by using quine McClusky method
$f(A, B, C, D) = \Sigma m\,(0, 1, 2, 3, 10, 11, 12, 13, 14, 15)$. (08 Marks)

2 a. Define an encoder. Design a priority encoder the truth table of which is shown in table Q2(a). The order of priority of inputs is $X_1 > X_2 > X_3$

Inputs				Outputs	
S	X_1	X_2	X_3	A	B
0	x	x	x	0	0
1	1	x	x	0	1
1	0	1	x	1	0
1	0	0	1	1	1
1	0	0	0	0	0

Table Q2(a) (06 Marks)

b. What is magnitude comparator? Write the truth table and circuit diagram of a 1 bit comparator. (06 Marks)

c. Mention different types of ROMS and explain each of them. (08 Marks)

3 a. Show the 8-bit addition of following decimal numbers into 2's compliment representation
i) +125 and – 68 ii) + 37 and – 115 iii) – 43 and – 78. (06 Marks)

b. What is a full adder? Give the truth table of full adder. From this truth table design a full adder circuit. (08 Marks)

c. Explain the working of a parallel adder. What are its advantages and disadvantages over a serial adder? (06 Marks)

4 a. What is a system clock? What are the characteristics of an ideal clock? (06 Marks)

b. Show how a D flip-flop can be converted to SR flip-flop. (06 Marks)

c. Explain the working of a JK flip-flop. Write its truth table, state diagram and excitation table. (08 Marks)

PART-B

5 a. Name and explain in short the four basic types of shift registers and draw a block diagram for each. (06 Marks)

b. Mention the differences between ripple and synchronous counters. (06 Marks)

c. Design a synchronous mod-3 counter with the following binary sequence using clocked JK flip-flops.
Counter sequence 0, 1, 2, 0, 1, 2. (08 Marks)

6 a. Write a note on Moore and Mealy models with respect [illegible] circuits. Compare the two models. [illegible]

b. Draw an ASM chart for a 2-bit counter [illegible] enabled) E = 0 (counting disabled). [illegible]

c. Reduce state transition diagram (Moor [illegible]
i) Row elimination method
ii) Implication table method.

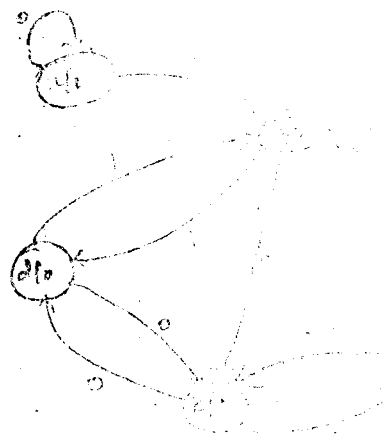

Fig. [illegible]

7 a. What is the binary ladder? Explain the binary ladder [illegible] ([illegible] Marks)

b. What is accuracy and resolution of the D/A converter? [illegible] D/A converter which uses a ladder network? If the full scale [illegible] converter is + 5V, what is the resolution in volts? ([illegible] Marks)

c. Explain continuous A/D conversion with an example. ([illegible] Marks)

8 a. What is a MOSFET? Explain its working. ([illegible] Marks)

b. Discuss the features of high speed TTL, low power TTL, [illegible] ([illegible] Marks)

c. Explain method for interfacing CMOS devices to TTL devices. ([illegible] Marks)

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06CS33

Third Semester B.E. Degree Examination, May/June 2010
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Simplify the given Boolean function by using K-map method and express it in SOP form. Realise logic circuit by using NAND gates only.
$f(A,B,C,D) = \sum(m(7, 9, 10, 11, 12, 13, 14, 15))$ **(06 Marks)**

b. Simplify following Boolean function by using K-map method in POS form:
$f(A,B,C,D) = \sum m(0,1,2,3,4,5,7)$ **(06 Marks)**

c. Find prime implicants for the Boolean expression by using Quine McClusky method.
$f(A,B,C,D) = \sum(1,3,6,7,8,9,10,12,14,15) + d(11,13)$ **(08 Marks)**

2 a. Define decoder. Draw logic diagram of 3:8 decoder with enable input. **(06 Marks)**

b. Implement the given Boolean function by using 8:1 multiplexer.
$f(A,B,C,D) = \sum(0,1,3,5,7,11,12,13,14)$ **(06 Marks)**

c. With a neat diagram, explain the decimal to BCD encoder. **(08 Marks)**

3 a. What are the three different models for writing a module body in verilog HDL? Give example for any one model. **(06 Marks)**

b. With truth table and a neat logic diagram, explain full adder implementation. **(06 Marks)**

c. Explain how IC 7483 can be used as 4 bit adder/subtractor. **(08 Marks)**

4 a. With transfer characteristic, explain how Schmitt trigger converts a random waveform into a rectangular waveform. **(06 Marks)**

b. Explain basic S.R flip-flop by using NOR gate. What is the drawback of S-R flip-flop? How J-K flip-flop is obtained from S-R flip-flop? **(08 Marks)**

c. Find out characteristic equations of J-K flip-flop and D flip-flop. **(06 Marks)**

PART – B

5 a. Explain any two types of shift register with waveforms. How Johnson counter is obtained from shift register? **(10 Marks)**

b. Design Mod-6 synchronous counter by using J-K flip-flop. Give excitation table of J-K flip-flop, state diagram and state transition table. **(10 Marks)**

6 a. Differentiate between Moore and Mealy model of synchronous sequential circuit. **(04 Marks)**

b. Reduce the state transition diagram of Mealy model by row elimination method and implication table method. **(16 Marks)**

State transition diagram.

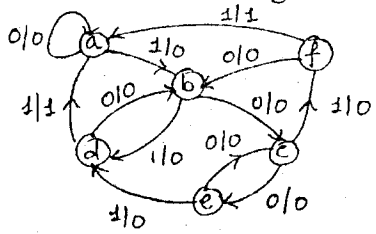

Fig. Q6 (b)

7 a. Explain with neat diagram, R-2R ladder type 4 bit D to A converter. Find out analog outp if input is 1100 and '1'=+5 volts. For 10 bit DAC if full scale output is 10.24 volts, what resolution? (10 Mark

b. Explain with a neat diagram, successive approximation type DAC. (10 Mark

8 a. With a neat circuit diagram, explain the operation of a two input TTL NAND gate wit tolem pole output. (08 Mark

b. Explain with a neat diagram, CMOS inverter. (06 Mark

c. Explain CMOS characteristics. (06 Mark

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